What is Claimed is:

1. A gate-body cross-linked metal-oxide-semiconductor transistor circuit comprising:

a first metal-oxide-semiconductor transistor having a gate, a source, a drain, and a body;

a second metal-oxide-semiconductor transistor have a gate, a source, a drain, and a body;

a first Schottky diode connecting the body of the first metal-oxide-semiconductor transistor to the gate of the second metal-oxide-semiconductor transistor; and

a second Schottky diode connecting the body of the second metal-oxide-semiconductor transistor to the gate of the first metal-oxide-semiconductor transistor.

2. The gate-body cross-linked metal-oxide-semiconductor transistor circuit defined in claim 1 wherein the first Schottky diode comprises an anode formed from the body of the first metal-oxide-semiconductor transistor and a cathode connected to the gate of the second metal-oxide-semiconductor transistor.

3. The gate-body cross-linked metal-oxide-semiconductor transistor circuit defined in claim 1 wherein:

the first Schottky diode comprises an anode formed from the body of the first metal-oxide-semiconductor transistor and a cathode connected to the

gate of the second metal-oxide-semiconductor transistor; and

the second Schottky diode comprises an anode formed from the body of the second metal-oxide-semiconductor transistor and a cathode connected to the gate of the first metal-oxide-semiconductor transistor.

4. The gate-body cross-linked metal-oxide-semiconductor transistor circuit defined in claim 1 further comprising an inverter that receives a control signal and provides a corresponding complement of the control signal, wherein the control signal is applied to the gate of the first metal-oxide-semiconductor transistor while the complement of the control signal is applied to the gate of the second metal-oxide-semiconductor transistor.

5. The gate-body cross-linked metal-oxide-semiconductor transistor circuit defined in claim 1 further comprising a silicon-on-insulator substrate having a silicon layer formed on a buried oxide layer, wherein the silicon layer is used to form the bodies of the first and second metal-oxide-semiconductor transistors.

6. The gate-body cross-linked metal-oxide-semiconductor transistor circuit defined in claim 1 wherein the drain of the first metal-oxide-semiconductor transistor and the drain of the second metal-oxide-

semiconductor are connected to each other.

7. The gate-body cross-linked metal-oxide-semiconductor transistor circuit defined in claim 1 further comprising a pull-up circuit having an output terminal, wherein the drain of the first metal-oxide-semiconductor transistor and the drain of the second metal-oxide-semiconductor transistors are both connected to the pull-up circuit output terminal.

8. The gate-body cross-linked metal-oxide-semiconductor transistor circuit defined in claim 1 wherein:

the Schottky diodes each have a cathode formed from a layer of metal; and

the bodies of the first and second metal-oxide-semiconductor transistors comprise silicon that is directly connected the layers of metal in the cathodes of the Schottky diodes.

9. A gate-body cross-linked metal-oxide-semiconductor transistor circuit formed on a silicon-on-insulating substrate, comprising:

a first metal-oxide-semiconductor transistor having a gate, a source, a drain, and a body;

a second metal-oxide-semiconductor transistor have a gate, a source, a drain, and a body;

a first Schottky diode having an anode formed from the body of the first metal-oxide-

semiconductor transistor and a cathode connected to the gate of the second metal-oxide-semiconductor transistor;

a second Schottky diode having an anode formed from the body of the second metal-oxide-semiconductor transistor and a cathode connected to the gate of the first metal-oxide-semiconductor transistor; and

circuitry that applies a signal to the gate of the first metal-oxide-semiconductor transistor while applying the complement of that signal to the gate of the second metal-oxide-semiconductor transistor.

10. The gate-body cross-linked metal-oxide-semiconductor transistor circuit defined in claim 9 further comprising:

a first input connected to the source of the first metal-oxide-semiconductor transistor;

a second input connected to the source of the second metal-oxide-semiconductor transistor; and

an output connected to both the drain of the first metal-oxide-semiconductor transistor and the drain of the second metal-oxide-semiconductor transistor.

11. The gate-body cross-linked metal-oxide-semiconductor transistor circuit defined in claim 9 further comprising:

a first input connected to the source of the first metal-oxide-semiconductor transistor;

a second input connected to the source of the second metal-oxide-semiconductor transistor;

an output connected to both the drain of the first metal-oxide-semiconductor transistor and the drain of the second metal-oxide-semiconductor transistor; and

a pull-up circuit connected to the output.

12. A gate-body cross-linked metal-oxide-semiconductor transistor circuit, comprising:

a first and second inputs;

an output;

a first metal-oxide-semiconductor transistor having a gate, first and second source-drain terminals, and a body, wherein the first source-drain terminal of the first metal-oxide-semiconductor transistor is connected to the first input and wherein the second source-drain terminal of the first metal-oxide-semiconductor transistor is connected to the output;

a second metal-oxide-semiconductor transistor having a gate, first and second source-drain terminals, and a body, wherein the first source-drain terminal of the second metal-oxide-semiconductor transistor is connected to the second input and wherein the second source-drain terminal of the second metal-oxide-semiconductor transistor is connected to the output;

a first Schottky diode having an anode formed from the body of the first metal-oxide-semiconductor transistor and a cathode connected to the gate of the second metal-oxide-semiconductor transistor;

a second Schottky diode having an anode formed from the body of the second metal-oxide-semiconductor transistor and a cathode connected to the gate of the first metal-oxide-semiconductor transistor; and

circuitry that applies a signal to the gate of the first metal-oxide-semiconductor transistor while applying the complement of that signal to the gate of the second metal-oxide-semiconductor transistor.

13. The gate-body cross-linked metal-oxide-semiconductor transistor circuit defined in claim 12 wherein the circuitry that applies the signal comprises an inverter that receives a control signal and provides its complement to the gate of the second metal-oxide-semiconductor transistor.

14. The gate-body cross-linked metal-oxide-semiconductor transistor circuit defined in claim 13 further comprising a silicon-on-insulator substrate having a silicon layer formed on a buried oxide layer, wherein the silicon layer is used to form the bodies of the first and second metal-oxide-semiconductor transistors.

15. The gate-body cross-linked metal-oxide-semiconductor transistor circuit defined in claim 14 further comprising a pull-up circuit connected to the output terminal.